

# Electrical Design Considerations

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## Proof Test

The purpose of "Proof Testing" Thermal Clad substrates is to verify that no defects reside in the dielectric material. Because testing requires that voltages be above the onset of partial discharge, we recommend the number of "Proof Tests" be kept at a minimum.

The term "Partial Discharge" includes a broad spectrum of life reducing (i.e. material damaging) phenomena such as:

1. Corona discharge
2. Treeing and surface contamination
3. Surface discharges at interfaces, particularly during fault induced voltage reversal
4. Internal discharges in voids or cavities within the dielectric



*"Proof Test" fixture to test multiple number of finished circuit boards at one time.*

The purpose of the "Proof Test" is to verify that there has been no degradation of the dielectric insulation due to the fabrication process or any material defects. Continued testing at these voltage levels will only take away from the life of the dielectric on the circuit board. It has been repeatedly verified that "Proof Testing" above the inception of partial discharge (700 Vac or 1200 Vac with proper use of solder-mask) will detect any and all defects in the dielectric isolation in the Thermal Clad circuit board. Any micro-fractures, delaminations or micro-voids in the dielectric will breakdown or respond as a short during the test.

The use of a DC "Proof Test" is recommended, from an operator safety standpoint. The voltage levels typically used are 1500 to 2250 VDC. Due to the capacitive nature of the circuit board construction, it is necessary to control the ramp up of the voltage to avoid nuisance tripping of the failure detect circuits in the tester and to maintain effective control of the test. This is to avoid premature surface arcing or voltage overshoot. There is safety consideration when DC testing, in that the operator must verify the board tested is fully discharged, prior to removing from the test fixture. A more detailed discussion of "Proof Test" is available upon request.

## Breakdown Voltage

The ASTM definition of dielectric breakdown voltage is: the potential difference at which dielectric failure occurs under prescribed conditions in an electrical insulating material located between two electrodes. This is permanent breakdown and is not recoverable. ASTM goes on to state that the results obtained by this test can seldom be used directly to determine the dielectric behavior of a material in an actual application. This is not a test for "fit for use" in the application, as is the "Proof Test," which is used for detection of fabrication and material defects to the dielectric insulation.

## Leakage Current HiPot Testing

Due to the variety of dielectric types, thicknesses and board layouts, not all boards test alike. All insulated metal substrates closely resemble a parallel plate capacitor during HiPot testing. Capacitance is equal to:

$$C = \epsilon A/d$$

where:

- $\epsilon$  = Permittivity (Dielectric Constant)
- A = Surface Area
- d = Distance (Dielectric Thickness)

The capacitance value changes with different configurations of materials and board layouts. This can be demonstrated where one board fails the test and another passes, but when both are actually tested for dielectric strength and leakage current in a controlled environment, both pass. Therefore, it is very important to properly design the testing and test parameters with the material characteristics in mind. Test set-up and parameters that over-stress or do not consider reactance of the material and its capacitive and resistive components, can lead to false failures and/or test damage of the board.

Another test characteristic that is generally misunderstood with insulated metal substrates is the leakage and charge current that take place during the test. In most cases, the leakage current value on insulated metal substrates is much smaller than the measurement capability of a typical HiPot tester. What is most misunderstood is the charge current that takes place during the test. Leakage current measurements can only be realized once the board has been brought to the full test voltage (DC voltage) and is held at that voltage during the test. This current value and rate  $dI/dT$  is directly related to the capacitance of the board. Therefore, a board that has an effective capacitance higher than another board will have a higher charge current rate than the one with a lower effective capacitance. This does not reflect the leakage current or the voltage withstand of the dielectric insulation instead, it represents the characteristic transient response of the dielectric. Therefore, one is not able to determine comparable leakage current based on the instantaneous charge current. For accurate leakage test data, bring the board up to full DC test voltage and hold.

## Creepage Distance And Discharge

Creepage distance and discharge has to be taken into account because Thermal Clad dielectrics often incorporate a metal base layer. Circuit board designers should consider "Proof Testing" requirements for: conductor-to-conductor and conductor-to-circuit board edge or through holes. The graphs below depict flashover: without soldermask, with soldermask and under oil.

